In re Patent Application of
ERRATICO
Serial No. **09/899,573**
Filed: **07/05/2001**
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REMARKS

The Examiner is thanked for the thorough examination of the present application. The specification has been amended to correct a minor typographic error. Independent Claims 12, 17, and 22 have been amended to more clearly define the subject matter thereof over the prior art, and to correct a minor typographical error therein. Support for the amendments may be found on pages 8-9 and 15-16 of the originally filed specification, for example. No new matter is being added.

In view of the amendments and the supporting arguments presented in detail below, it is submitted that all of the claims are patentable.

I. The Claimed Invention

The present invention is directed to an integrated structure. As recited in amended independent Claim 17, for example, the integrated structure includes a substrate having a first conductivity type and an epitaxial layer on the substrate. The epitaxial layer has the first conductivity type and a conductivity less than a conductivity of the substrate. Moreover, the integrated structure also includes first and second regions in the epitaxial layer each having a second conductivity type opposite the first conductivity type. The first and second regions extend from a surface of the epitaxial layer opposite the substrate into the epitaxial layer to form respective first and second junctions therewith. Moreover, first and second electrodes are also included for independently biasing the first and second junctions, respectfully.

Further, the integrated structure also includes an isolating element positioned between the first and the second regions and extending from the surface of the epitaxial layer at least as far as a top surface of the substrate for reducing an injection of current through said epitaxial layer from said first region to said second region when the first and second junctions are oppositely biased. The isolating element partially surrounds at least one of the first and second regions. Furthermore, the isolating element also terminates above a bottom surface of the substrate. Independent Claims 12 and 22 are directed to related integrated structures and have similarly been amended to recite first and second electrodes for independently biasing the first and second junctions, respectfully, and that the isolating elements thereof are for

reducing an injection of current through the epitaxial layer from the first region to the second region when the first and second junctions are oppositely biased.

II. The Claims Are Patentable

The Examiner rejected independent Claims 12 and 17 over Boden, Jr., and also rejected independent Claim 22 over Boden, Jr. in view of Nakagawa. Boden Jr. is directed to a high voltage MOS-gated device which includes a plurality of DMOS transistors which share a common source electrode **39** and common drain electrode **40** (see FIG. 1 of Boden, Jr.). More particularly, P-type base diffusion strips **15-18** are formed in an N- epitaxial layer **12**, and trenches **49-51** are formed between pairs of the base diffusion strips. The trenches **49-51** are then filled with semi-insulating polysilicon (SIPOS) **48**, **52**, **53** to reduce on-resistance of the device.

It may be seen in FIG. 1 of Boden, Jr. that a junction is formed between each of the P base diffusion strips on either side of the trenches **49-51** and the N- epitaxial layer **12**. Because all of the P base diffusion strips **15-18** share the common electrode **39**, the junctions formed thereby on both sides of each trench **49-51** will always be biased in the same manner. That is, Boden, Jr., fails to teach or fairly suggest first and second electrodes for independently biasing these junctions. Accordingly, no current can be injected from one of these junctions to the other through the epitaxial layer **12**.

Indeed, the trenches described in Boden, Jr. are not for reducing an injection of current through the epitaxial layer from a first region to a second region when the first and second junctions are oppositely biased. Rather, the trenches have a completely different function, namely to cause depletion regions in the epitaxial layer **12** during blocking

conditions. See, e.g., col. 2, lines 56-65 of Boden, Jr. To do so, the trenches are connected to a conducting electrode **79** (see FIG. 3 of Boden, Jr.), and these trenches cannot function as isolating elements as recited in the above-noted independent claims since no current is injected through the epitaxial layer **12** when the above-noted junctions are oppositely biased.

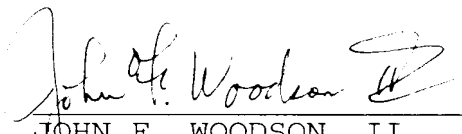
Thus, neither Boden, Jr. nor the combination of Nakagawa (or any of the remaining prior art of record) therewith teaches or fairly suggests all of the recitations of the above noted independent claims. Rather, there cannot be any motivation or suggestion to so modify these references because to selectively modify the electrode configuration of the Boden, Jr. device to produce the claimed invention would not only change the principle of operation thereof, but also render it unsatisfactory for its intended purpose. To find otherwise would require the impermissible use of the claimed invention in hindsight as a roadmap or template to piece together the teachings of the prior art.

Accordingly, it is submitted that independent Claims 12, 17, and 22 are patentable over the prior art. Their respective dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the amendments to the claims and the arguments presented above, it is submitted that all of the claims are patentable. Accordingly, a Notice of Allowance is respectfully requested in due course. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,



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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: DIRECTOR, U.S. PATENT AND TRADEMARK OFFICE, BOX AF, WASHINGTON, D.C. 20231, on this 22nd day of April, 2003.

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